REMARKS

Claims 7-10 and 17-20 are pending in the present application. Claims 1-6, 11-16, and 21-30 have been withdrawn from consideration. Claims 7-10 and 17-20 stand rejected under 35 USC §102(b). Claims 7 and 17 have been amended.

The Applicant appreciates the Examiner's thorough examination of the subject application and respectfully request reconsideration of the subject application based on the above amendments and the following remarks.

35 U.S.C. § 102(b) REJECTIONS

The Examiner has again rejected claims 7-10 and 17-20 under 35 USC § 102(b) as being anticipated by U.S. Patent Number 5,173,792 to Matsueda ("Matsueda" or the "Matsueda Reference"). The Applicant respectfully traverse these rejections for the reasons provided below.

Matsueda teaches an electro-optical display with a redundancy system "wherein two TFTs 140A and 140B and two signal lines X_{2m-1} and X_{2m} are provided per display element." Matsueda, col. 15, lines 9-13. Referring to FIG. 11 of Matsueda, an MOS capacitor 170 having three portions 170A, 170B, and 170C is connected to the pixel electrode 141 through a single hole 165. See, e.g., Id., col. 15, lines 25-30. Respective drains 144 and 174 to each of the TFTs 140A and 140B are connected to the driving electrode 141 via a single contact hole 162 and 163, respectively. See, e.g., Id., col. 15, lines 55-58. Accordingly,

> [w]hen either TFT 140A and 140B is to be electrically isolated due to a defect, the cutoff is accomplished at position 154 or position 155, as the case may be, and, correspondingly, a storage capacitor that is likewise to be electrically isolated, the cutoff is accomplished at position 151, 152, or 153, as the case may be, via laser trimming or other such known treatment.

Id., col. 15, lines 62-68. The Examiner asserts that, the "pixel electrode 141, which is connected to the drain electrode, should be or act like an extension of the drain electrode." The Applicants respectfully disagree.

In claims 7 and 17 of the present invention, two electrodes (electrodes at two portions) "are disposed in parallel at two different portions on an extension portion of the drain electrode" and "said electrodes disposed in parallel are connected to the pixel electrodes via through holes which are respectively formed in a layer insulating film, which is on said electrodes, and stacked via the auxiliary capacitance electrode and insulating film so as to respectively form the storage capacitances."

> Consequently, in the liquid crystal display panel 30 of the liquid crystal display device, when either one of the two connection electrode 5a and the branch-side connection electrode 33, and the auxiliary capacitance electrode 11a are short-circuited, a leak defect can be mended by laser-cutting either the drain thin line portion 31 or the drain branch thin line portion 32 leading to the connection electrode 5a or the branch-side connection electrode 33 on the short-circuited side off, and further, by electrically separating the connection electrode 5a or the branch-side connection electrode 33 on the short-circuited side from the pixel electrode 7.

Specification, page 48, lines 9-20 (Emphasis added). Thus, according to the present invention, leakage can be corrected by isolating the electrode 5a or 33 from the drain electrode 5 by cutting one of the drain thin line portion 31 or the drain branch thin line portion 32 and, further, by isolating the electrode 5a or 33 from the pixel 7 by separating the connection electrode 5a or the branch-side connection electrode 33 from the pixel electrode 7 on the short circuit side.

In addition, as described above, even when thus making a correction in which the electrode on the short-circuited side and the pixel electrode are electrically disconnected, the other electrode is still in contact with the pixel electrode, thereby enabling a pixel electrode in that portion to remain electrically connected to the drain electrode. As a result, it is possible to easily correct leaking defects between the

auxiliary capacitance electrode and the drain electrode and between the source wiring and the drain electrode, thereby normalizing pixels. See, e.g., Id., page 11, lines 2-21.

The Matseuda reference does not teach, mention or suggest providing two cutoffs to prevent leakage. Matsueda merely discloses an arrangement in which a plurality of electrodes to be connected to pixel electrodes is formed on an auxiliary capacitance electrode, with an insulating film being provided between the plurality of electrodes and the auxiliary capacitance electrode. In Matsueda, the drain electrodes 144 and 174 have no "extension portion of the drain electrode" that corresponds to the drain thin line portion 31 and/or the drain branch thin line portion 32 of the present invention. The driving electrode 141 therefore corresponds to the "pixel electrodes" of the present invention and not to "an extension portion of the drain electrode" as asserted by the Examiner.

Moreover, the drain electrodes 144 and 174, pixel electrode 141, and MOS capacitors 170 are serially connected in that order in Matsueda. In contrast, with the invention as claimed, the "drain electrode", the "extension portion of the drain electrode", and the "pixel electrodes" are serially connected in this order. Thus, the electrical connections between the Matsueda reference and the present invention differ.

According to amended claims 7 and 17, the insulating film also is "on said electrodes." Thus, the "extension portion of the drain electrode" (and the electrodes thereon), the "layer insulating film", and the "pixel electrodes" are provided separately. More specifically, the "extension portion of the drain electrode" and the "pixel electrodes" are separate entities. As a result, the Matsueda reference completely lacks an "extension portion of the drain electrode."

Finally, in Matsueda, one pixel electrode in the display region is connected to two TFTs and a plurality of storage capacitors to optimize the size of the capacitors that are cut off, which attains a transmittance that is the same as the transmittance of normal pixels. In contrast, with the present invention, normalization of pixels is

attained by easily correcting leaking defects between the auxiliary capacitance electrode and the drain electrode and between the source wiring and the drain electrode. Therefore, Matsueda and the present invention differ in terms of the effects and the problems solved.

Accordingly, it is respectfully submitted that, the rejected claims are not anticipated and/or made obvious by the Matsueda reference, and further, satisfy all of the requirements of 35 U.S.C. 100, et seq., especially § 102(b). Accordingly, claims 7-10 and 17-20 are allowable. Moreover, it is respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

If for any reason a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge or credit Deposit Account No. **04-1105**.

Respectfully submitted,

Date: November 5, 2003

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